DELAY LINE AND TRANSISTOR WITH RE DELAY GATE

ABSTRACT OF THE DISCLOSURE

A method and apparatus for implementing trimming circuits. More particularly, embodiments of the present invention provide a transistor that supplies sufficient current to trim a trimming fuse when the transistor is powered up and after it receives a select signal at its gate. When the trimming fuse is trimmed, it decouples undesired electrical connections in a circuit. Also provided is a delay structure that adds an RC delay to the select signal. The RC delay is of a sufficiently long duration so as to decrease the switching speed of the transistor. The delay structure also provides a pass filter to filter power and voltage spikes in the select signal.